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The illustrated brief application of defect distribution model for heterojunction device by admittance spectroscopy

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ABSTRACT

The dielectric properties of the devices can be studied by using admittance spectroscopy (AS). Majority carrier traps are experimentally analyzed without sophisticated mathematical manipulation. Experimental evidence obtained from AS of the devices may display several features that cannot be explained by the usual single RC circuits representing a depleted junction region and undepleted bulk elements. In this study, ac behavior of typical pn junction diode is simulated using temperature depended AS in a broad frequency range (5 Hz to 13 MHz). The frequency-dependent admittance data of typical pn junction has been discussed based on a discrete deep or shallow trap model. The analytically obtained frequency depended $-dC/d\omega$ and $\tan\delta$ (loss tangent) curves are peaks function. The position of the peak depends on the temperature and dc-bias. This peak position gives us information about deep or shallow trap states. The trapping time and trap energy levels can be deduced from $-dC/d\omega$ versus ω or $\tan\delta$ versus ω curves. This investigation shows that suitable complex admittance measurement data obtained during the capacitance–voltage measurement process are used to calculate the trapping time and energetic position of the traps. A theoretical analysis and computer simulation are presented in order to illustrate the nature of the trap and the technique by which accurate trapping time and energy position of the trap state can be obtained.

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1. Introduction

The study of ac transport properties of the devices yields supplement and complementary data on doping densities, capture cross section and activation energy for electrically active defects in semiconductor devices. The preferred method for determining these parameters is AS.

AS spectroscopy has recently been performed on Schottky and MIS diode structures for investigation of the interface state density [1–3]. AS also can be performed on heterojunction diode structures such as CdS/p-Si, CdZnS/p-GaAs, GaP/ZnO, CdTe/ZnTe and InP/GaInAs. When a small ac voltage is applied across the sample, the response of the system is entirely characterized by complex admittance $Y(\omega)$, which is a function of oscillator frequency (ω). $G(\omega)$ and $B(\omega)$ are real and imaginary parts of $Y(\omega)$, respectively. The real and imaginary parts of $Y(\omega)$ are related to each other by the Kramers–Kronig relations and each of them requires full spectral information. AS probes the frequency and temperature dependence of the capacitance $C(\omega, T)$ of a rectifying junction. The principle of AS is to probe interaction of an external field with the electric dipole moment of the sample. Obtained data are expressed by Bode plot or Nyquist plot. Temperature and frequency dependent conductance loss peak measurement is the basis of AS.

The frequency dispersion in the depletion region is due to traps. If the time constant τ of the trap is comparable to the inverse frequency of the small signal, the trap makes contribution to the total capacitance and the peak of the conductance curve along the frequency axis becomes visible. It is well known that the capture and emission processes are controlled by trap characteristics. A heterojunction diode structure can be mimicked by a capacitor the dielectric loss of which may exhibit low or high values, depending on the nature of trap levels in the depletion region.

One of the parameters of a dielectric material is the loss tangent. The loss tangent characterizes dissipation of electromagnetic energy in a dielectric material. The angle between the resistive (lossy) component of an electromagnetic field and its reactive (lossless) component in the complex plane represents loss tangent term. The frequency dependency of dielectric loss is sensitive to various rate processes such as capture and emission process in deep/shallow levels in the space charge region.

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Energy dissipation and storage processes are modeled in an AS equivalent circuit by a resistance and capacitance, respectively.

The junction capacitance is generally known as capacitance of space-charge-region (C_{scr}). If there is electronically active traps in the space-charge-region (SCR) of the device, capacitance spectrum is affected at lower frequencies and/or higher temperatures. Hole or electron traps within the SCR are charged and discharged depending on applied frequency. Evaluation of capacitance spectrum of a device allows us to determine the distribution of traps.

There are plenty of publications in the literature about interface state density distribution in some diode structures [1–6]. There are many different kinds of models that have been adopted into measurement analysis by many researchers for more than three decades [7–11]. Most of them followed the approach of Card and Rhoderick [10] and Hill–Coleman [11] to extract interface state density. The calculated interface state density can be considered as two-dimensional density of state. However, there is a model which is very feasible and ingenious for heterojunction device structure because it gives three-dimensional density of trap state distribution by applying a simple mathematical procedure [12]. Its feasibility depends on a requirement of only frequency dependent capacitance values. It does not require any measured frequency versus conductance data. However, most of the researchers are not aware of the existence of T. Walter et al.'s works; hence, they used Card and Rhoderick, Hill–Coleman model for every device structure. Therefore, this article focused on how this model can be useful to determine not only three-dimensional density of trap states distribution but also shallow or deep energy levels in a heterojunction diode structure.

As a result, it is important to find out which analyzing technique can be used to obtain shallow or deep levels correctly in heterojunction device structure. The main purpose of this article is to determine the best approximate method to analyze shallow or deep levels by conducting a theoretical simulation of AS curves of heterojunction devices. Computer simulation study is performed by different circuit models for shallow and deep trap levels in heterojunction device structure. Our obtained results are comparable with those in some earlier works.

2. Theory

In this part, a theoretical simulation of AS will be conducted to analyze shallow and deep levels. During the simulation, an equivalent circuit model has been suggested to describe the device structure. An equivalent circuit model is constructed as the junction dynamic resistance (R_d) parallel to the trap capacitance (C_{trap}) and C_{scr}, connected to the serial heterojunction diode trap resistance (R_{trap}). The problem can be demonstrated with the illustration in Fig. 1, which is an accurate representation of the one-sided p-Si/CdS heterojunction diode and a reasonable approximation to the case of discrete bulk traps. C_{scr} represents the capacitance due to the depletion region while the combination of C_{trap} and R_{trap} describe the effect of the traps whose characteristic time constant (τ). $\tau = R_{trap}C_{trap}$ gives rise to a loss tangent peak when $\omega = l/\tau$. The parallel dynamic resistance, R_d, describes the leakage path that often accompanies heterojunction devices and can physically arise from generation-recombination currents within the SCR, native defects across the p type semiconductor, or leakage due to periphery effects. Electronically active traps in the SCR make contribution to the capacitance spectrum of the junction. The capacitance, which includes the contribution of carrier trap to the C_{scr}, is represented by measured capacitance (C_m). $C_m(\omega)$ can be written as,

$$C_m(\omega) = C_{scr} + \frac{C_{trap}}{(1+(R_{trap}/R_d))^2 + (C_{trap}R_{trap}\omega)^2}, \tag{1}$$

if $R_d \gg R_{trap}$ then $C_m(\omega)$ reduces to;

$$C_m(\omega) = C_{scr} + \frac{C_{trap}}{1+(\omega C_{trap}R_{trap})^2}. \tag{2}$$

We can approximate to Eq. (2) to take into account some cases given below. At low frequencies measured capacitance values can be represented as; $C_{LF} = \lim_{\omega\to 0} C_m(\omega)$,

$$C_{LF} = \lim_{\omega\to 0}\left[C_{scr} + \frac{C_{trap}}{1+(\omega C_{trap}R_{trap})^2}\right] \approx C_{scr} + C_{trap}. \tag{3}$$

Then C_{trap} can be written as;

$$C_{trap} = C_{LF} - C_{scr}, \tag{4}$$

$$C_m(\omega) = C_{scr} + \frac{C_{LF} - C_{scr}}{1+(\omega C_{trap}R_{trap})^2}. \tag{5}$$

Eq. (5) is in well agreement with Ref. [13] and shows that our approximation is consistent with previous studies in the literature.

Electronically active defects are easily analysed by using suitably obtained temperature dependent C–f (capacitance–frequency) data [14–20]. The effects of trap levels to the device capacitance are obviously represented by the humps on the capacitance curves. These humps are useful for calculating trapping time constant ($\tau = R_{trap}C_{trap}$). For a small concentration of traps ($N_{acceptor} \ll N_{trap}$), the τ approaches the value $\tau = 1/\omega_I$, where ω_I is the inflection frequency of the electronic transition [12]. Point on the graph of $C(\omega)$ where the concavity changes from flat-to-down is called inflection point of the graph of $C(\omega)$. The following result connects the concept of inflection points to the derivatives properties of the function: if $dC/d\omega|_{\omega=\omega_I}$ exists and $d^2C/d\omega^2|_{\omega=\omega_I}$ changes sign at $\omega = \omega_I$, then the point (ω_I, $C(\omega_I)$) is an inflection point of the graph of $C(\omega)$. If $d^2C/d\omega^2|_{\omega=\omega_I}$ exists at the inflection point, then $d^2C/d\omega^2|_{\omega=\omega_I} = 0$. This particular angular frequency, ω_I, corresponds to the angular emission frequency for the traps. The critic inflection frequency can be written in the form;

$$\omega_I = \frac{1+(R_{trap}/R_d)}{\tau\sqrt{3}}. \tag{6}$$

Another way to obtain the trap information is frequency depended loss tangent measurement. Loss tangent is expressed in terms of admittance component, which is given elsewhere;

$$\tan\,\delta(\omega) = \frac{G(\omega)}{\omega C(\omega)}. \tag{7}$$

The unknown component is conductance in Eq. (7).

We can easily derive the conductance by writing equivalent admittance for suggested equivalent circuit in Fig. 1. The conductance component can be written as;

$$G_m(\omega) = \frac{a_1 + a_2\omega^2}{a_1^2 + a_3\omega^2}, \tag{8}$$

where

$$a_1 = R_{trap} + R_d, \tag{8.a}$$

$$a_2 = R_{trap}R_d^2C_{trap}^2, \tag{8.b}$$

$$a_3 = R_{trap}^2R_d^2C_{trap}^2. \tag{8.c}$$

By applying Eq. (8) to Eq. (7), the loss tangent function yields as;

$$\tan\,\delta(\omega) = \frac{a_1 + a_2\omega^2}{a_4\omega + a_5\omega^3}, \tag{9}$$

where

$$a_4 = C_{trap}R_d^2 + C_{scr}(R_d + R_{trap})^2, \tag{9.a}$$

$$a_5 = C_{scr}R_{trap}^2R_d^2C_{trap}^2. \tag{9.b}$$

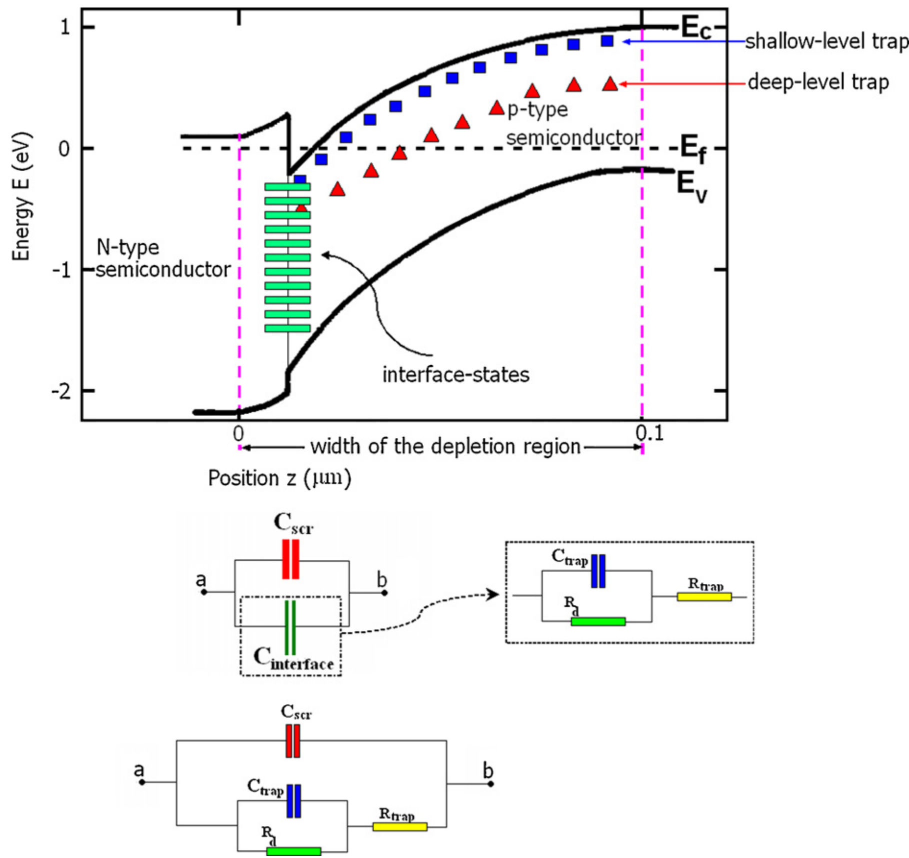

Fig. 1. Energy band diagram and equivalent circuit for a one-sided p/N heterojunction diode. The band gaps of the two materials are not exactly to scale.

The loss tangent function has two extrema points. The trapping time of the device can also be calculated from one of the extrema in the frequency domain. For the condition of device R_d value is quite larger then R_{trap} ($R_d \gg R_{trap}$), one can simplify the extrema point equation as given below;

$$\omega_{peak} = \frac{1}{\tau}\sqrt{1+\frac{C_{trap}}{C_{scr}}}. \tag{10}$$

In this study, a useful method to acquire trap energy distribution by using admittance measurement data was suggested. This method consists of calculating the derivation of the frequency dependent capacitance data along with scaling the frequency into an energy axis.

The energetic position of the trap can be calculated by using a famous formulation that was derived by *T*. Walter et al. [12]. Angular frequency (ω) data have to be turned into an energy values by using the formula $E_\omega = (k_B T E_{00}/(E_{00} - k_B T))\ln(\xi_{00}T^2/\omega)$ [21]. In addition, it is found that the pre-exponential factor, ξ_{00}, depends on the energetic depth of the trap (E_a) with respect to the corresponding band edge according to Meyer–Neldel rule [22], where ξ_{00} and E_{00} are constants for related processes [12,13,20–29]. Energy distribution of traps $N_t(E_\omega)$ depends on the derivative of C_m with respect to angular frequency ω, built-in potential V_{bi}, band gap E_g, probing energy level E_ω, Boltzmann constant k_B and temperature T;

$$N_t(E_\omega) = -\frac{2V_{bi}^{3/2}\sqrt{q}}{Ak_B T w\sqrt{qV_{bi}-(E_g-E_\omega)}}\left(\omega\frac{dC_m}{d\omega}\right). \tag{11}$$

3. Results and discussion

In this study, simulations are performed under consideration of one-sided (p-Si/CdS heterojunction) Si based solar cells. C–ω characteristics of the device were obtained for only one shallow trap level located at 260 meV at the temperature range of 150–300 K (Fig. 2). The value of the trap level energy that is used during the simulation process has been given in the literature [30,31].

The capacitance values of the device are constant under a critical measurement frequency and this constant value is equal to C_{LF} at 300 K. Capacitance curves display an inflection at a critical frequency for all the measurement temperatures as seen in Fig. 2. The frequency dependent capacitance spectra exhibit an evident

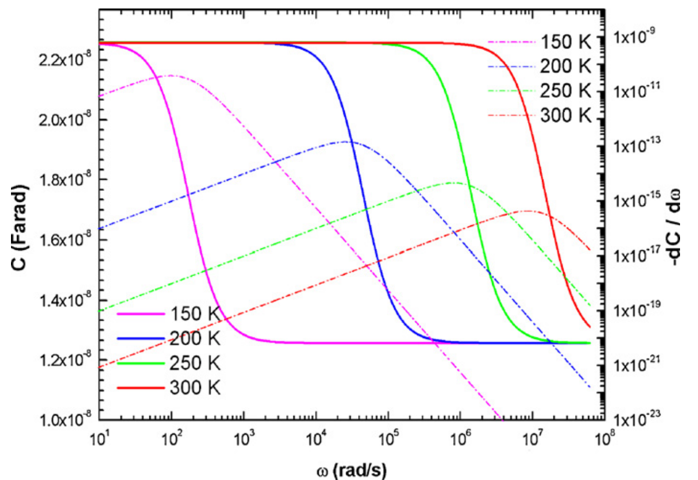

Fig. 2. Capacitance and differentiated capacitance spectra at different temperatures under 0 V dc bias for shallow trap level. The position of the peak shifts significantly with temperature. C_{trap}/C_{scr} = 0.79. This value is obtained by iterative simulation process.

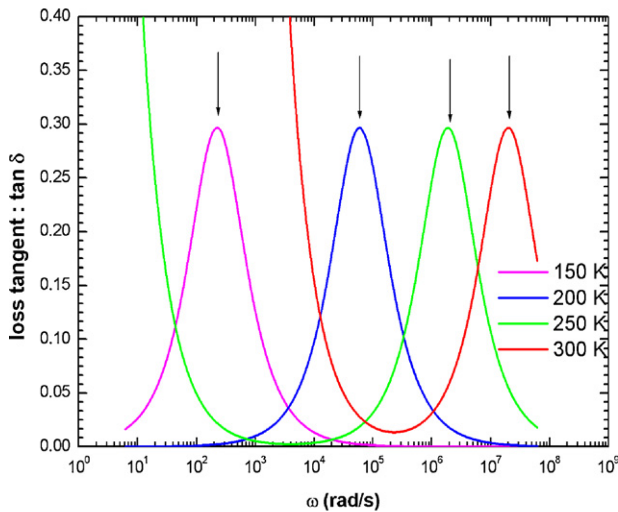

Fig. 3. tan δ versus ω spectra of device at different temperatures under 0 V dc bias for shallow trap level. The position of the peak shifts significantly with temperature. C_{trap}/C_{scr} = 0.79.

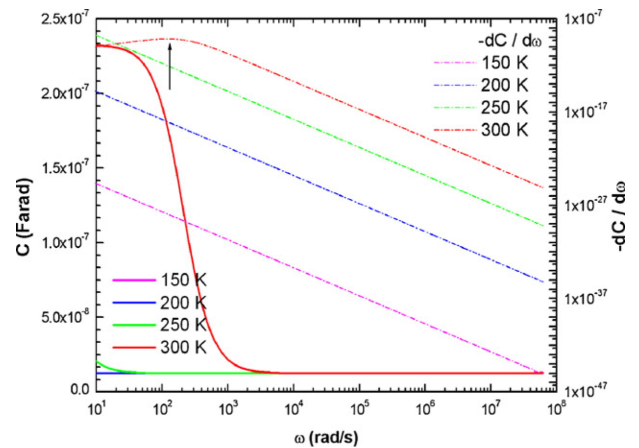

Fig. 4. Capacitance $C(\omega)$ and differentiated capacitance spectra of $dC/d\omega$ at different temperatures under 0 V dc bias for deep trap level. C_{trap}/C_{scr} = 39.76. This value is obtained by iterative simulation process.

step due to discreet distribution of defects. This critical inflection frequency shifts to lower frequency with decreasing temperature due to temperature dependence of the time constant of the device. At the higher measurement frequencies ($f > 10^8$ Hz), the capacitance at all temperatures is assumed to be constant and nearly equal to C_{scr}.

A simple method to obtain the energy distribution of defects by using admittance data was suggested in the previous section. Admittance data are simulated by considering typical solar cell based on p-type c-Si. The suggested method consists of derivation of the capacitance with respect to frequency. The energy range between 100 meV and 1 eV in the band gap can be investigated by varying the temperature from 150 K to 300 K and the frequency from 1 Hz to 10^8 Hz. As can be seen in Fig. 2, the differentiated capacitance spectra ($dC/d\omega$ versus ω) displays a peak function. The peak position shifts to higher frequencies with increasing temperature according to the temperature dependence of the τ. In addition, the peaks in the differentiated capacitance curve have Gaussian characteristic. The Gaussian peak looks like a characteristic in the shape of "bell curve".

tan δ–ω characteristics are simulated for only one shallow trap level (260 meV) in investigated device structure at the temperature range of 150–300 K. As can be seen in Fig. 3, tan δ versus ω characteristic of simulated device structure displays a single peak. Thus, the equivalent circuit can be designed as a single τ ($R_{trap}C_{trap}$) for every temperature. Peak position slides to higher frequencies with increasing temperature due to temperature dependence of the τ. These advocate that interface components could play a reasonably concerned role for the ac conduction.

The same parameters were considered for the deep trap level simulation procedure. Simulated C–ω characteristic of the investigated device structure at various temperatures ranging from 150 to 300 K for only one deep trap level (560 meV) is given in Fig. 4. During the simulation process, the considered trap level energy was taken from the early relevant literature [30–34].

As can be seen in Fig. 2, the $C(\omega)$ spectra for the shallow trap level show a pronounced step at the temperatures lower than 300 K. The dispersion in case of the deep trap level is displayed in Fig. 4. Step like behavior is obviously observed at only 300 K. As seen in Fig. 4, at low measurement frequencies ($\omega \leq 40$ rad/s) the capacitance is assumed to be constant, which is nearly equal to $40 \times C_{scr}$, and exhibits flat response at the frequency region of 10^3 rad/s < ω < 10^8 rad/s for 300 K. At the higher measurement frequencies ($\omega > 10^3$ rad/s), the capacitances at all temperatures are assumed to be constant and nearly equal to C_{scr}. The frequency dependent capacitance characteristics exhibit a rather pronounced step at 300 K due to deep trap level. Only high temperature frequency dependent capacitance measurement is advisable to detect deep level because the ω_I value outstands for the temperatures higher than 250 K. As seen in Fig. 4, the features in the differentiated capacitance spectra ($dC/d\omega$ versus ω) at 300 K exhibit a peak function and this peak disappears at lower temperatures ($T < 300$ K) due to the temperature dependency of the τ.

At 300 K operating temperature, tan δ versus ω plot of simulated device structure yields a single peak at about 10^3 rad/s as depicted in Fig. 5. Thus, it is concluded that the equivalent circuit can be constructed as a single τ ($R_{trap}C_{trap}$) time constant for every temperature. As can be seen in Fig. 5 tan δ spectra exhibit a peak function and this peak could only be detectable at 300 K. It is already proven in theoretical part that this critical peak is directly related with temperature dependency of the τ of semiconductor material. $C(\omega)$–ω and tan δ–ω characteristics manifest that the device capacitance measured at room temperature is largely dominated by contributions from trap levels in the band gap regardless of whether trap level is deep or shallow.

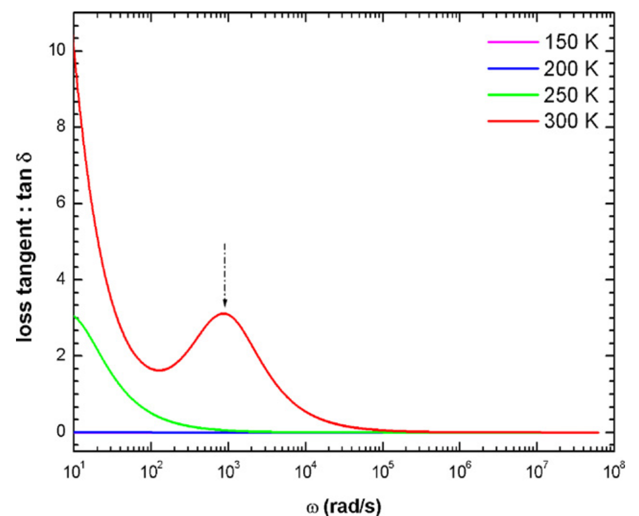

Fig. 5. Simulated tan δ–ω characteristic of the investigated device structure at various temperatures ranging 150–300 K for only one deep trap level (560 meV). C_{trap}/C_{scr} = 39.76.

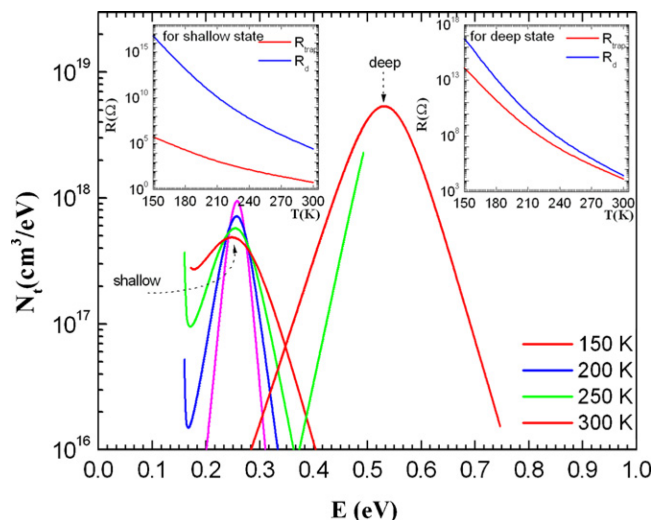

Fig. 6. Defect distribution of the simulated device structure for shallow and deep trap situation. Parameters were considered for the deep and shallow level simulation process are: $\nu_0 = 10^{11}$ s^{-1} (attempt to escape frequency), $\sigma = 10^{-15}$ cm^2 (capture cross section), $A = 0.42$ cm^2, $W = 0.35$ μm (depletion width), $N_A = 10^{16}$ cm^{-3} (acceptor concentration), $V_{bi} = 0.9$ V.

AS was finally utilized to investigate the energetic distribution of defects in the depletion region of the typical solar cell. The frequency dependency of the device capacitance at zero bias for different temperatures has been shown in Figs. 2 and 4. The contribution of the deep and shallow levels to the device capacitance especially at high temperatures and low frequencies is clearly reflected in the humps of the capacitance curves. These humps in the capacitance characteristics move forward to higher frequencies with increasing temperature due to the temperature dependency of the τ.

$C(\omega)$–ω values may be translated into a distribution of the density of states by taking the derivative of the capacitance with respect to the frequency and may be re-scaling the frequency axis into an energy axis [13–16]. Fig. 6 displays density of states distribution of considered typical solar cell device in this study. The resulting density of state distributions at different temperatures is shown in Fig. 6 (at left and right side) for the shallow and deep trap, respectively. Calculation parameters are given in Fig. 6 caption. Carrier density, built-in voltage (V_{bi}) and dielectric constant were chosen by assuming abrupt junction approximation. Space charge width (w) of the junction is calculated from 0 V dc bias capacitance value.

It is known that the distribution of traps creates detrimental effect on device operation performance. The presence of a deep and shallow trap level makes it difficult to extract the deep trap energy level from frequency depended capacitance measurements, even if a probing frequency is chosen, at which the ac occupation of the deep/shallow centers cannot follow. Deep traps are only detectable at high temperatures ($T > 250$ K) because of R_{trap} exhibits quite high values at low temperatures. When the circuit has high R_{trap} values, so that an interface element is nearly an open circuit situation in AC analysis. In such a case, the circuit response consists of only C_{scr}. Therefore, we could not observe any defect distribution at lower temperatures.

Shallow trap level distribution of device is seen at left hand side of Fig. 6. All curves follow each other at all-operating temperatures. The pronounced step in the $C(\omega)$ curves of the device (Fig. 2) corresponds to the defect peak at 260 meV (Fig. 6). $C(\omega)$ curves of the deep trap level device are dominated by a dispersion only at higher temperatures ($T > 250$ K), which is reflected in a broader defect distribution. Careful comparison of the density of states of the simulated device between 260 meV and 560 meV suggests a shift among the curves for different temperatures, pointing to temperature dependency of R_{trap} and R_d as inserted two figures in Fig. 6. It is also worth mentioning that these deep states were only observed in materials containing high R_{trap} and high C_{trap} values. This suggests that the physical origins of these trap levels are closely related with semiconductor nature because temperature dependent R_{trap} values exhibit semiconductor behavior.

4. Conclusions

In this study, the trap distribution in the device is evaluated by theoretical analysis and computer simulation. It is shown that the presence of electronically active traps can be displayed by using AS. τ and energetic position of trap can be easily calculated from $C_m(\omega)$ data. AS is a very useful tool to detect deep and shallow levels in semiconductor device and there is a plenty of detailed work studying how to detect interface state density or trap levels by AS [14–19,24,26,27,29]. However, there is not enough detailed work to study how to detect shallow and deep levels by AS with an illustrative way for heterojunction devices [13,21,22,29]. Thus, it became necessary to carry out that kind of study. The aim of the present article is to demonstrate a method to analyze shallow and deep levels in heterojunction devices by conducting a theoretical simulation of AS curves of shallow and deep levels. During the theoretical simulation, an equivalent circuit model consisting of the heterojunction C_{scr}, C_{trap}, R_{trap} and the R_d has been adopted at the temperature range from 150 K to 300 K. The evaluation scheme consists of calculation of the derivative of the frequency dependency of the capacitance accompanied by scaling the frequency into an energy axis. The shallow (260 meV) and deep trap (560 meV) levels are simulated using $C(\omega)$–ω and tan δ–ω characteristics. Computer simulation study of the shallow and deep trap levels is performed by this method, the results verify that this method works quite well. Temperature dependent R_{trap} and C_{trap} values determine the energetic trap distribution of the device. We conclude that the deep trap energy level can be observable at higher temperatures for typical Si based device. However, the shallow trap energy level can rather be observable at all temperatures.

References

[1] F. Yakuphanoglu, J. Alloys Compd. 507 (2010) 184.
[2] S. Altindal, H. Uslu, J. Appl. Phys. 109 (2011) 074503.
[3] S. Altindal, H. Kanbur, I. Yücedag, A. Tataroglu, Microelectron. Eng. 85 (2008) 1495.
[4] Ö. Vural, Y. Safak, A. Türüt, S. Altindal, J. Alloys Compd. 513 (2012) 107.
[5] K.S. Kim, R.K. Gupta, G.S. Chung, F. Yakuphanoglu, J. Alloys Compd. 509 (2011) 10007.
[6] V. Rajagopal Reddy, M. Siva Pratap Reddy, B. Prasanna Lakshmi, A. Ashok Kumar, J. Alloys Compd. 509 (2011) 8001.
[7] A.M. Cowley, S.M. Sze, J. Appl. Phys. 36 (1965) 3212.
[8] C.R. Crowell, H.B. Shore, E.E. LaBate, J. Appl. Phys. 36 (1965) 3843.
[9] C.R. Crowell, S.M. Sze, Solid-State Electron. 9 (1966) 1035.
[10] H.C. Card, E.H. Rhoderick, J. Phys. D: Appl. Phys. 4 (1971) 1589.
[11] W.A. Hill, C.C. Coleman, Solid State Electron. 23 (1980) 987.
[12] T. Walter, R. Herberholz, C. Müller, H.W. Schock, J. Appl. Phys. 80 (1996) 4411.
[13] A. Jasenek, U. Rau, V. Nadenau, H.W. Schock, J. Appl. Phys. 87 (2000) 594.
[14] G.S. Chung, K.S. Kim, F. Yakuphanoglu, J. Alloys Compd. 507 (2000) 508.
[15] H. Uslu, A. Bengi, S.Ş. Çetin, U. Aydemir, Ş. Altındal, S.T. Aghaliyeva, S. Özçelik, J. Alloys Compd. 507 (2010) 190.
[16] R. Ranjan, R. Kumar, N. Kumar, B. Behera, R.N.P. Choudhary, J. Alloys Compd. 509 (2011) 6388.
[17] M.K. Hudait, S.B. Krupanidhi, Solid-State Electron. 44 (2000) 1089.
[18] A.A.M. Farag, A. Ashery, E.M.A. Ahmed, M.A. Salem, J. Alloys Compd. 495 (2010) 116.
[19] A. Bengi, H. Uslu, T. Asar, Ş. Altındal, S.Ş. Çetin, T.S. Mammadov, S. Özçelik, J. Alloys Compd. 509 (2011) 2897.
[20] D.L. Losee, J. Appl. Phys. 46 (1975) 2204.
[21] R. Herberholz, M. Igalson, H.W. Schock, J. Appl. Phys. 83 (1998) 318.
[22] R. Herberholz, T. Walter, C. Müller, T. Friedlmeier, H.W. Schock, M. Saad, M.Ch. Lux-Steiner, V. Alberts, Appl. Phys. Lett. 69 (1996) 2888.

[23] Zs.J. Horváth, L. Dózsa, O.H. Krafcsik, T. Mohácsy, Gy. Vida, Appl. Surf. Sci. 234 (2004) 67.
[24] A. Singh, Solid-State Electron. 28 (1985) 223.
[25] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, third ed., John Willey & Sons, New York, 2007.
[26] S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. 49 (1986) 85.
[27] A. Gümüş, A. Türüt, N. Yalçin, J. Appl. Phys. 91 (2002) 245.
[28] H. Bayhan, A.S. Kavasoğlu, Sol. Energy 80 (2006) 1160.
[29] J. Osvald, Zs.J. Horváth, Appl. Surf. Sci. 234 (2004) 349.
[30] S.K. Pang, A.W. Smith, A. Rohatgi, IEEE Trans. Electron. Dev. 42 (1995) 662.
[31] O. Breitenstein, P. Altermatt, K. Ramspeck, M.A. Green, J. Zhao, A. Schenk, Conference Record of the 2006, IEEE 4th World Conference on Photovoltaic Energy Conversion, vol. 1, 2006, p. 879.
[32] C. Gong, N. Posthuma, F. Dross, E. Van Kerschaver, F. Giovanni, G. Beaucarne, J. Poortmans, R.J.O.M. Hoofman, Photovoltaic Specialists Conference PVSC'08. 33rd IEEE, 2008, p. 1.
[33] K. Wünstel, P. Wagner, Solid State Commun. 40 (1981) 797.
[34] M. Kaniewska, M. Lal, Sol. Energy Mater. Sol. Cells 72 (2002) 509.